REMARKS

Claims 1, 7-9, 15-17, 19, 29, and 30 have been amended, and claims 1-2, 7-10, 15-20, and 29-30 are pending in the present application. The claim amendments are supported by the specification as originally filed, with no new matter being added. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

1. Rejections Under 35 U.S.C. § 112

Claims 15 and 29-30 have been rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not sufficiently described in the specification. In addition, claims 15 and 29-30 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicants respectfully traverse.

The Office Action indicated that there is not support in the specification for the passivation layer including a nitrogen-containing silane, and that such a limitation is unclear. Claims 15 and 29-30 have been amended to delete the terms "nitrogen-containing silane" from these claims, and now recite that the passivation layer comprises nitrogen.

Thus, Applicants respectfully request that the rejections of claims 15 and 29-30 under 35 U.S.C. § 112 be withdrawn.

2. Rejections Under 35 U.S.C. § 102

Claims 1, 9, 17, and 19 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,861,675 to Sasaki et al. (hereinafter "*Sasaki*") for the reasons stated on pages 3-5 of the Office Action. Applicants respectfully traverse.

Claim 1 has been amended to recite that the passivation layer comprises "the chemical structure M-N-H_x, where M represents the metal of the interconnect" and that "the passivation layer substantially covers the upper surface of the interconnect in order to chemically protect about 1-1,000 atomic lattice layers thereof." Support for these recitations in claim 1 can be found in the application as filed on page 10, lines 4-9.

There is no teaching or suggestion in *Sasaki* of a passivation layer comprising the chemical structure M-N-H_x, and that a passivation layer chemically protects about 1-1,000 atomic lattice layers of an interconnect. Rather, *Sasaki* discloses that a tungsten nitride film containing fluorine is formed as a barrier in the contact hole of a semiconductor device.

Independent claim 9 has been amended to recite that "the passivation layer substantially covers the upper surface of the metallic first structure in order to chemically protect about 1-1,000 atomic lattice layers thereof." Similarly, independent claims 17 and 19 have been amended to recite that "the first and second passivation layers substantially cover the upper surface of the interconnect in order to chemically protect about 1-1,000 atomic lattice layers thereof." There is no teaching or suggestion in *Sasaki* of such features as recited in claims 9, 17, and 19.

Accordingly, for the above reasons, claims 1, 9, 17, and 19 are not anticipated by *Sasaki*. Applicants therefore respectfully request that the rejection of these claims under 35 U.S.C. § 102(e) be withdrawn.

3. Rejections Under 35 U.S.C. § 103

Claims 1-2, 7-10, and 16-20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,780,908 to Sekiguchi et al. (hereinafter "*Sekiguchi*") in view

of U.S. Patent No. 6,077,774 to Hong et al. (hereinafter "*Hong*") for the reasons set forth on pages 5-6 of the Office Action. In addition, claims 1-2, 7-10, and 16-20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Sekiguchi* in view of U.S. Patent No. 6,114,238 to Liao (hereinafter "*Liao*") for the reasons set forth on pages 6-7 of the Office Action. Applicants respectfully traverse.

As discussed previously, claim 1 has been amended to recite that the passivation layer comprises the chemical structure M-N-H_x, and that the passivation layer chemically protects about 1-1,000 atomic lattice layers of the interconnect. Independent claims 7, 8, 9, 16, 17, and 19 recite the similar features of the passivation layer(s) chemically protecting about 1-1,000 atomic lattice layers of the interconnect. There is no teaching or suggestion in *Sekiguchi*, *Hong*, or *Liao* of such recited features for a passivation layer(s).

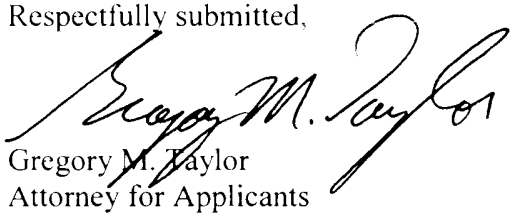
Accordingly, for the above reasons, claims 1, 7-9, 16-17, and 19, as well as dependent claims 2, 10, 18, and 20, would not have been obvious over the cited references. Applicants therefore respectfully request that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the present claims. In the event the Examiner finds any remaining impediment to the prompt allowance of this application, which could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 27th day of December 2002.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW THE CHANGES MADE

IN THE CLAIMS:

Claims 1, 7-9, 15-17, 19, 29, and 30 have been amended as follows:

1. (Four Times Amended) A semiconductor structure comprising:

an electrically conductive interconnect disposed within a first dielectric layer, said electrically conductive interconnect having an upper surface and comprising a metal;

a passivation layer [disposed] upon said upper surface, said passivation layer comprising the chemical structure M-N-H_x, where M represents the metal of the interconnect [nitrogen adsorbed upon said upper surface according to Brunauer's Type V adsorption]; and

an interlayer dielectric [disposed] upon said first dielectric layer and upon said upper surface, said interlayer dielectric being continuously adhered to said upper surface;

wherein the passivation layer substantially covers the upper surface of the interconnect in order to chemically protect about 1-1,000 atomic lattice layers thereof.

7. (Four Times Amended) A semiconductor structure comprising:

an electrically conductive interconnect having an upper surface and being disposed within a dielectric layer, said electrically conductive interconnect including:

a titanium liner layer disposed within a depression in said dielectric layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer and filling said depression;

a first passivation layer comprising a tungsten nitride compound and being disposed upon said upper surface;

a second passivation layer comprising multiple layers of nitrogen compounds adsorbed upon said first passivation layer according to Brunauer's Type V adsorption; and

an interlayer dielectric disposed upon said dielectric layer and upon said upper surface, said interlayer dielectric being continuously adhered to said upper surface;

wherein the first and second passivation layers substantially cover the upper surface of the interconnect in order to chemically protect about 1-1,000 atomic lattice layers thereof.

8. (Four Times Amended) A semiconductor structure comprising:

an electrically conductive interconnect disposed within a dielectric layer, said electrically conductive interconnect having an upper surface and including:

a titanium liner layer disposed within a depression in said dielectric layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer and filling said depression;

a passivation layer [disposed] upon said upper surface and comprising nitrogen adsorbed upon said upper surface according to Brunauer's Type V adsorption; and

an interlayer dielectric [disposed] upon said dielectric layer and upon said upper surface, said interlayer dielectric being continuously adhered to said upper surface;

wherein the passivation layer substantially covers the upper surface of the interconnect in order to chemically protect about 1-1,000 atomic lattice layers thereof.

9. (Four Times Amended) An interconnect in an electronic device comprising:

a metallic first structure disposed within a first silicon oxide layer, said metallic first structure having an upper surface;

a passivation layer [disposed] upon said upper surface, said passivation layer formed by exposing said upper surface to a plasma consisting essentially of a nitrogen-containing silane; and

a second silicon oxide layer disposed upon said first silicon oxide layer and upon said upper surface, said second silicon oxide layer being continuously adhered to said upper surface;

wherein the passivation layer substantially covers the upper surface of the metallic first structure in order to chemically protect about 1-1,000 atomic lattice layers thereof.

15. (Four Times Amended) An interconnect in an electronic device comprising:

a metallic structure disposed within a first silicon oxide layer, said metallic structure having an upper surface and including:

a titanium liner layer disposed within an interconnect corridor in said first silicon oxide layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer;

a first passivation layer disposed upon said upper surface and comprised of a tungsten nitride compound;

a second passivation layer [consisting essentially of a nitrogen-containing silane] comprising nitrogen disposed upon said first passivation layer; and

a second silicon oxide layer disposed upon said first silicon oxide layer and upon said upper surface, said second silicon oxide layer being continuously adhered to said upper surface;

wherein the first and second passivation layers substantially cover the upper surface of the interconnect in order to chemically protect about 1-1,000 atomic lattice layers thereof.

16. (Four Times Amended) An interconnect in an electronic device comprising:

a metallic structure disposed within a first silicon oxide layer, said metallic structure having an upper surface and including:

a titanium liner layer disposed within an interconnect corridor in said first silicon oxide layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer;

a passivation layer disposed upon said upper surface and formed by exposing said upper surface to a plasma consisting essentially of a nitrogen-containing silane; and

a second silicon oxide layer disposed upon said first silicon oxide layer and upon said upper surface, said second silicon oxide layer being continuously adhered to said upper surface;

wherein the passivation layer substantially covers the upper surface of the metallic structure in order to chemically protect about 1-1,000 atomic lattice layers thereof.

17. (Thrice Amended) A semiconductor structure comprising:

an electrically conductive interconnect disposed within a first dielectric layer, said electrically conductive interconnect having an upper surface;

a first passivation layer disposed upon said upper surface, said first passivation layer comprising a tungsten nitride compound;

a second passivation layer comprising multiple layers of nitrogen compounds adsorbed upon said first passivation layer according to Brunauer's Type V adsorption; and

an interlayer dielectric disposed upon said first dielectric layer and upon said upper surface, said interlayer dielectric being continuously adhered to said upper surface;

wherein the first and second passivation layers substantially cover the upper surface of the interconnect in order to chemically protect about 1-1,000 atomic lattice layers thereof.

19. (Thrice Amended) An interconnect in an electronic device comprising:

a metallic first structure disposed within a first silicon oxide layer, said metallic first structure having an upper surface;

a first passivation layer disposed upon said upper surface, said first passivation layer comprising a tungsten nitride compound;

a second passivation layer comprising multiple layers of nitrogen compounds adsorbed upon said first passivation layer according to Brunauer's Type V adsorption; and

a second silicon oxide layer disposed upon said first silicon oxide layer and upon said upper surface, said second silicon oxide layer being continuously adhered to said upper surface;

wherein the first and second passivation layers substantially cover the upper surface of the interconnect in order to chemically protect about 1-1,000 atomic lattice layers thereof.

29. (Twice Amended) A semiconductor structure comprising:

an electrically conductive interconnect disposed within a first dielectric layer, said electrically conductive interconnect having an upper surface;

a passivation layer disposed upon said upper surface, said passivation layer comprising nitrogen [consisting essentially of a nitrogen-containing silane]; and

an interlayer dielectric disposed upon said first dielectric layer and upon said upper surface, said interlayer dielectric being continuously adhered to said upper surface;

wherein the passivation layer substantially covers the upper surface of the interconnect in order to chemically protect about 1-1,000 atomic lattice layers thereof.

30. (Twice Amended) A semiconductor structure comprising:

an electrically conductive interconnect disposed within a first dielectric layer, said electrically conductive interconnect having an upper surface;

a first passivation layer upon said upper surface, said first passivation layer comprising a tungsten nitride compound;

a second passivation layer upon said first passivation layer, said second passivation layer comprising nitrogen [consisting essentially of a nitrogen-containing silane]; and

an interlayer dielectric disposed upon said first dielectric layer and upon said upper surface, said interlayer dielectric being continuously adhered to said upper surface;

wherein the first and second passivation layers substantially cover the upper surface of the interconnect in order to chemically protect about 1-1,000 atomic lattice layers thereof.